REMARKS

STATUS OF THE CLAIMS

In accordance with the foregoing, claims 1, 2, 4-8, 11-20, 22-26 and 29-36 are amended for format and formality purposes and no new features for the claimed invention are added. Claims 37-48 were previously cancelled. Claims 3, 9, 10, 21, 27, 28 were previously withdrawn. Claims 1, 2, 4-8, 11-20, 22-26 and 29-36 are pending and under consideration.

No new matter is being presented, and approval of the amended claims is respectfully requested.

CHANGES IN THE SPECIFICATION

On pages 2-3, items 2-4, of the Action, the Title and the Abstract are objected to as not being clearly indicative of the invention to which the claims are directed. Therefore, the Title is amended and the Abstract is replaced in its entirety herein to comply with all requirements set forth in the MPEP. Approval of the Title and Abstract are respectfully requested.

REJECTIONS OF CLAIMS 1-2, 4-8, 11-13, 15 AND 17 UNDER 35 U.S.C. §102(b) AS BEING ANTICIPATED BY LEEDY (U.S. PATENT NO. 5,103,557)

The rejections of claims 1-2, 4-8, 11-13, 15 and 17 are respectfully traversed and reconsideration is requested.

The present invention, as recited in independent claim 1, is characterized in that the displacement of the position of each electric component formed on each individual board is detected relative to the design position of the electronic component before it is covered with an insulating layer. Furthermore, design data to be used for processing the board after it is covered with the insulating layer is dynamically corrected using the detected displacement. After the design data is dynamically corrected as described above, the thus corrected data is used in the maskless exposure.

Since the design data necessary for the maskless exposure and the via formation can be corrected dynamically for each individual board, each individual electronic component and each terminal of the electronic component, optimum maskless exposure, and optimum via formation, is achieved.

In contrast, Leedy discloses testing transistors or logic units on an integrated circuit wafer prior to interconnect metallization, using a specially fabricated flexible tester surface. The probe points electrically contact the contacts of the wafer by fluid pressure. Then, the interconnect metallization is laid down and patterned under control of a CAD computer system. (Abstract).

The portions of Leedy cited by the Examiner disclose merely *aligning* the wafer 1 with the test surface 10, so that the logic units on the wafer 1 can be tested. The results of the test are used to modify a net list t produce a database for the desired interconnect patters on the wafer 1. (See column 5, lines 1-15, and column 6, lines 45-64). In other words, if a defective ICLU or transistor is found, the interconnects are arranged so as to bypass the defective ICLU and interconnect a defect-free ICLU from the stock of redundant ICLUs. (See column 5, lines 33-43).

Therefore, Leedy fails to teach or even suggest detecting the position of an *individual electronic component*, and calculating a displacement *between the design position of the electronic component and the actual position of said first electronic component* on the surface of said board, and holding said displacement as first displacement data, as recited in independent claim 1.

Thus, it is respectfully submitted that independent claim 1, as well as the dependent claims, patentably distinguish over the prior art.

REJECTIONS OF CLAIMS 19-20, 22-26 AND 29-36 UNDER 35 U.S.C. §103(a) AS BEING UNPATENTABLE OVER LEEDY IN VIEW OF KULKARNI ET AL. (U.S. PATENT NO. 5,991,699)

Independent claim 19 recites capturing, before said board is covered with a first insulating layer, an image of a surface of said board on which a first electronic component is formed; calculating a displacement between the design position of said first electronic component and the actual position of said first electronic component detected from first image data obtained by imaging the surface of said board, and holding said displacement as first displacement data; and correcting, based on said first displacement data, design data to be used for processing said board after said board is covered with said first insulating layer.

Therefore, for at least the reasons provided above for independent claim 1, it is respectfully submitted that independent claim 19, as well as the dependent claims, patentably distinguishes over the prior art.

Further, Kulkarni et al. is merely cited as disclosing identifying defects and issuing corrective actions and imaging means. Therefore, it is respectfully submitted that Kulkarni et al.

fails to teach or suggest the features of independent claims 1 and 19 described above.

REJECTIONS OF CLAIMS 14, 16 AND 18 UNDER 35 U.S.C. §103(a) AS BEING UNPATENTABLE OVER LEEDY IN VIEW OF KULKARNI ET AL.

Claims 14, 16 and 18 depend from independent claim 1 and inherit the patentability thereof. Thus, it is respectfully submitted that claims 14, 16 and 18 patentably distinguish over the prior art for at least the reasons noted above for claim 1.

Further, as stated above, it is submitted that Kulkarni et al. fails to teach or suggest the features of independent claim 19 and therefore also the similarly-recited features of independent claim 1, as described above.

CONCLUSION

In accordance with the foregoing, it is respectfully submitted that all outstanding objections and rejections have been overcome and/or rendered moot. Further, all pending claims patentably distinguish over the prior art. There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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